

Yasutoshi HIRANO, S.N. 09/955,885
Page 2

IDkt. No. 2271/65888

Listing of Claims

1. (previously presented) A signal processing apparatus comprising:
a digital signal processor comprising an internal memory part storing a program to be executed;
an external memory part storing programs executable in said digital signal processor;
a clock signal generating part generating a clock signal and outputting the clock signal to said digital signal processor; and
a clock signal control part controlling outputting of said clock signal to said digital signal processor so that said programs stored in said external memory part can be forwarded to said internal memory part,
wherein the control of output of the clock signal is performed without requiring reinitialization of said digital signal processor.

2. (original) The signal processing apparatus as claimed in claim 1, wherein said clock signal control part forwards said programs read from said external memory part to said internal memory after stopping outputting said clock signal to said digital signal processor.

3. (original) The signal processing apparatus as claimed in claim 1, wherein said clock signal control part comprises a forward circuit part and a clock control part, said clock control part stops outputting said clock signal to said digital signal processor after said forward circuit part supplies said clock control part with a signal requesting that said clock control part stops outputting said clock signal to said digital signal processor so that said programs stored in said

Yasutoshi HIRANO, S.N. 09/955,885
Page 3

Dkt. No. 2271/65888

external memory part can be forwarded to said internal memory part.

4. (original) The signal processing apparatus as claimed in claim 3, wherein said clock control part restarts outputting said clock signal to said digital signal processor after said forward circuit part supplies said clock control part with a signal requesting that said clock control part outputs said clock signal to said digital signal processor when said programs stored in said external memory part are completely forwarded to said internal memory part.

5. (original) The signal processing apparatus as claimed in claim 1, wherein said clock signal control part controls outputting of said clock signal to said digital signal processor in compliance with a request from said digital signal processor.

6. (original) The signal processing apparatus as claimed in claim 1, wherein said clock signal control part controls outputting of said clock signal to said digital signal processor in compliance with a request from an outside of said signal processing apparatus.

7. (original) The signal processing apparatus as claimed in claim 1, wherein said clock signal control part comprises a forward circuit for forwarding a desired part of said programs read from said external memory part to said internal memory.

8. (previously presented) A modem for modulating/demodulating a communication data by using a signal processing apparatus comprising:

a digital signal processor comprising an internal memory part storing a program to be

Yasutoshi HIRANO, S.N. 09/955,885
Page 4

Dkt. No. 2271/65888

executed;

an external memory part storing programs executable in said digital signal processor;
a clock signal generating part for generating a clock signal and outputting the clock signal to said digital signal processor; and
a clock signal control part controlling outputting of said clock signal to said digital signal processor so that said programs stored in said external memory part can be forwarded to said internal memory part,

wherein the control of output of the clock signal is performed without requiring reinitialization of said digital signal processor.

9. (original) The modem as claimed in 8, wherein said clock signal control part forwards said programs read from said external memory part to said internal memory after stopping outputting said clock signal to said digital signal processor.

10. (original) The modem as claimed in 8, wherein said clock signal control part comprises a forward circuit part and a clock control part, said clock control part stops outputting said clock signal to said digital signal processor after said forward circuit part supplies said clock control part with a signal requesting that said clock control part stops outputting said clock signal to said digital signal processor so that said programs stored in said external memory part can be forwarded to said internal memory part.

11. (original) The modem as claimed in 10, wherein said clock control part restarts

Yasutoshi HIRANO, S.N. 09/955,885
Page 5

Dkt. No. 2271/65888

outputting said clock signal to said digital signal processor after said forward circuit part supplies said clock control part with a signal requesting that said clock control part outputs said clock signal to said digital signal processor to said clock control part, after said programs stored in said external memory part are completely forwarded to said internal memory part.

12. (original) The modem as claimed in 8, wherein said clock signal control part controls outputting of said clock signal to said digital signal processor in compliance with a request from said digital signal processor.

13. (original) The modem as claimed in 8, wherein said clock signal control part controls outputting of said clock signal to said digital signal processor in compliance with a request from an outside of said signal processing apparatus.

14. (original) The modem as claimed in 8, wherein said clock signal control part comprises a forward circuit for forwarding a desired part of said programs read from said external memory part to said internal memory.